

Notice of References Cited	Application/Control No. 10/621,449	Applicant(s)/Patent Under Reexamination MATSUI ET AL.	
	Examiner Helen Rossoshek	Art Unit 2825	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,135,647 A	10-2000	Balakrishnan et al.	716/18
*	B	US-6,175,946 B1	01-2001	Ly et al.	716/4
	C	US-			
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	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

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	U	Tabbara et al.; "Fast hardware-software co-simulation using VHDL models"; 9-12 March 1999; Design, Automation and Test in Europe Conference and Exhibition 1999. Proceedings; Page(s):309 - 316
	V	Bhattacharya et al.; "An RTL methodology to enable low overhead combinational testing"; 17-20 March 1997; European Design and Test Conference, 1997. ED&TC 97. Proceedings; Page(s):146 - 152
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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